



Logic Synthesis and Verification (The Springer International Series in Engineering and Computer Science)

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Research and development of logic synthesis and verification have matured considerably over the past two decades. Many commercial products are available, and they have been critical in harnessing advances in fabrication technology to produce today's plethora of electronic components. While this maturity is assuring, the advances in fabrication continue to seemingly present unwieldy challenges.

Logic Synthesis and Verification provides a state-of-the-art view of logic synthesis and verification. It consists of fifteen chapters, each focusing on a distinct aspect. Each chapter presents key developments, outlines future challenges, and lists essential references.

Two unique features of this book are technical strength and comprehensiveness. The book chapters are written by twenty-eight recognized leaders in the field and reviewed by equally qualified experts. The topics collectively span the field.

Logic Synthesis and Verification fills a current gap in the existing CAD literature. Each chapter contains essential information to study a topic at a great depth, and to understand further developments in the field. The book is intended for seniors, graduate students, researchers, and developers of related Computer-Aided Design (CAD) tools.

From the foreword: "The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book. Their innovative work contributed to design automation tools that permanently changed the course of electronic design." by *Aart J. de Geus, Chairman and CEO, Synopsys, Inc.*

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